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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,518	07/23/2002	Tung-Cheng Kuo	MXIP0088USA	6631

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,518	KUO ET AL.	
	Examiner	Art Unit	
	Hoai V. Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4, 6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is responsive to communication(s) filed on March 3, 2004.

2. Claims 1-4, 6 and 7 are presented for examination

Allowability Withdrawn

3. The indicated allowability of claim 5 as merged into the amended claim 1 filed on March 3, 2004 is withdrawn in view of the newly discovered reference(s) to Hayashi et al. and Huang et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

> (e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1, 2, 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated Hayashi et al. US Pat. No. 5768184 (Paper No. 1203).

Figures 2-6, 14 and 16 of Hayashi are directed to a method for reading (col. 7, line 38 to col. 8, line 16) a non-volatile memory with multi-level output currents comprising: Figure 2 of Hayashi providing a memory cell (2) having a source (4, col. 6, line 1), a drain (4, col. 6, line 1), a channel (6, col. 5, line 29), a first isolation layer (8, col. 6, lines 2 and 3) positioned on the channel, a non-conducting dielectric layer comprising silicon nitride positioned on the first isolation layer (ONO, col. 6, lines 9 and 10 and col. 9, lines 14-20), a second isolation layer (12, col. 6, lines 8 and 9) and a conductor (14, col. 6, lines 12-15), source (col. 9, lines 14-17); applying a first reading voltage on a conductor of the memory cell (col. 7, lines 43 and 44); applying a second reading voltage on the drain (col. 7, lines 44 and 45) of the memory cell; and grounding the source (fig. 4) of the memory cell, thereby obtaining an output current (fig. 6); wherein the memory cell comprises a first programming state, a second programming state, a third programming state, or a fourth programming state, and the output current comprises a maximum output current corresponding the memory cell in the first programming state, a first output current corresponding to the memory cell second programming state, a second output

current corresponding to the memory cell in the third programming state, or a third output current corresponding to the memory cell in the fourth programming state (col. 7, lines 27-37. Also see col. 2, lines 20-29, col. 5, lines 28-50 and col. 9, lines 40-52).

6. Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated Huang et al. US Pat. No. 6643170.

As per claims 1, 2, 6 and 7, Figures 4-6 of Huang are directed to a method for reading (col. 3, lines 49-57) a non-volatile memory with multi-level output currents comprising: providing a memory cell (fig. 4) having a source (404/406), a drain (404/406), a channel (between 404 and 406 in 402), a first isolation layer (410) positioned on the channel, a non-conducting dielectric layer comprising silicon nitride positioned on the first isolation layer (412, col. 6, lines 9 and 10 and col. 2, lines 27-33), a second isolation layer (414) and a conductor (416) positioned on the second isolation layer; applying a first reading voltage on a conductor of the memory cell (col. 3, lines 43 and 44); applying a second reading voltage on the drain (col. 1, lines 36-38) of the memory cell; and grounding the source (col. 3, lines 36 and 37) of the memory cell, thereby obtaining an output current (Table 1); Table 1 in column 4 discloses wherein the memory cell comprises a first programming state, a second programming state, a third programming state, or a fourth programming state, and the output current comprises a maximum output current corresponding the memory cell in the first programming state, a first output current corresponding to the memory cell second programming state, a second output current corresponding to the memory cell in the third programming state, or a third output current corresponding to the memory cell in the fourth programming state (col. 4, lines 14-32).

As per claim 3, Figure 4 of Huang discloses wherein the non-conducting dielectric layer comprising a first region (418) nearby the drain and a second region (420) nearby the source.

As per claim 4, Table 1 in column 4 of Huang discloses wherein the first programming state represents that both the first region and the second region are not injected with electrons, the second programming state represents that the second region is not injected with electrons but the first region, the third programming state represents that the first region is not injected with electrons but the second region, and the fourth programming state represents that both the first region and the second region are injected with electrons (col. 4, lines 14-32).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. US Pat. No. 5768184 (Paper No. 1203) in view of Huang et al. US Pat. No. 6643170.

Hayashi discloses the non-conducting dielectric layer but fails to disclose wherein the non-conducting dielectric layer comprising a first region nearby the drain and a second region nearby the source in claim 3 and programming the first and second regions under various states in claim 4.

However, Huang discloses all limitations in claims 3 and 4 as shown in the 35 U.S.C. 102(e) rejections above. It would have been obvious to a person of ordinary skill in the art at the time invention was made to include the non-conducting dielectric layer comprising the first region nearby the drain and the second region nearby the source as taught by Huang. Because Huang suggests that wherein the non-conducting dielectric layer can locally trap a plurality of charges to form a plurality of charge trapping regions. The charges stored in these charge-trapping regions are a first bit of memory and a second bit memory. The charges that are stored in the trapping region as the second bit of memory form an electrical barrier. The level of the threshold current depends on the size of the electrical barrier. The different levels of the threshold currents are thereby used to define the different memory states of the multi-level memory (col. 2, lines 27-33). And moreover, an additional implantation process at the vicinity of the source/drain region is obviated in the multi-level memory cell. Only reading one side of the bit memory of the current flow between the source/drain regions is sufficient to determine memory state (col. 4, lines 37-41).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 308-4839. The examiner can normally be reached on Mon. - Thur. from 7:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phones number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 308-4839. The examiner can normally be reached on Mon. - Thur. from 7:00 A.M. to 5:30 P.M. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1777. Other inquiries of this application should be called to (571) 272-1562 or the fax number (703) 872-9306.

H. Ho
March 11, 2004

Hoai V. Ho
Primary Examiner
Art Unit 2818